

L Number	Hits	Search Text	DB	Time stamp
1	0	(mosfet adj model).ti.	USPAT	2004/07/09 13:03
2	1	(mosfet and model).ti.	USPAT	2004/07/09 13:04
3	10	BSIM3V3	USPAT	2004/07/09 13:04
4	371	diode near model	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/09 13:05
5	72	(diode near model) and mosfet	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/09 13:05
6	60	((diode near model) and mosfet) and parallel	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/09 13:49
7	277	(703/15).CCLS.	USPAT	2004/07/09 13:49
8	2	((703/15).CCLS.) and (mosfet adj model)	USPAT	2004/07/09 13:49

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

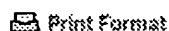
- ☐ By Author
- ☐ Basic
- ☐ Advanced

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE ANONYMOUS

- ☐ Access the IEEE Enterprise File Cabinet



Print Format

Your search matched **46** of **1049776** documents.A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:

You may refine your search by editing the current search expression or entering a new one in the text box.

mosfet <and> direct <and> tunneling <and> current <and>

Search

☐ Check to search within this result set

Results Key:

JNL = Journal or Magazine **CNF** = Conference **STD** = Standard**1 Edge hole direct tunneling leakage in ultrathin gate oxide p-channel MOSFETs***Kuo-Nan Yang; Huan-Tsung Huang; Ming-Jer Chen; Yeou-Ming Lin; Mo-Chiun Yu; Jang, S.S.A.; Yu, D.C.H.; Mong-Song Liang;*Electron Devices, IEEE Transactions on , Volume: 48 , Issue: 12 , Dec. 2001
Pages:2790 - 2795[\[Abstract\]](#) [\[PDF Full-Text \(152 KB\)\]](#) **IEEE JNL****2 MOSFET gate leakage modeling and selection guide for alternative gate dielectrics based on leakage considerations***Yee-Chia Yeo; Tsu-Jae King; Chenming Hu;*Electron Devices, IEEE Transactions on , Volume: 50 , Issue: 4 , April 2003
Pages:1027 - 1035[\[Abstract\]](#) [\[PDF Full-Text \(756 KB\)\]](#) **IEEE JNL****3 Scaling effects on gate leakage current***Watanabe, H.; Matsuzawa, K.; Takagi, S.;*Electron Devices, IEEE Transactions on , Volume: 50 , Issue: 8 , Aug. 2003
Pages:1779 - 1784[\[Abstract\]](#) [\[PDF Full-Text \(471 KB\)\]](#) **IEEE JNL****4 Modeling of direct tunneling gate current in ultra-thin gate oxide MOSFETs: a comparison between simulators***Cassan, E.; Galdin, S.; Dollfus, P.; Hesto, P.;*Simulation of Semiconductor Processes and Devices, 1999. SISPAD '99. 1999 International Conference on , 6-8 Sept. 1999
Pages:115 - 118[\[Abstract\]](#) [\[PDF Full-Text \(272 KB\)\]](#) **IEEE CNF****5 Effects of neglecting carrier tunneling on electrostatic potential in calculating direct tunneling gate current in deep submicron MOSFETs***Hakim, M.M.A.; Haque, A.;*

[\[Abstract\]](#) [\[PDF Full-Text \(230 KB\)\]](#) IEEE JNL

6 Direct tunneling gate leakage current in transistors with ultrathin silicon nitride gate dielectric

Yee Chia Yeo; Qiang Lu; Wen Chin Lee; Tsu-Jae King; Chenming Hu; Xiewen Wang; Xin Guo; Ma, T.P.;

Electron Device Letters, IEEE , Volume: 21 , Issue: 11 , Nov. 2000
Pages:540 - 542

[\[Abstract\]](#) [\[PDF Full-Text \(104 KB\)\]](#) IEEE JNL

7 A comparative study of gate direct tunneling and drain leakage currents in n-MOSFET's with sub-2 nm gate oxides

Yang, N.; Henson, W.K.; Wortman, J.J.;

Electron Devices, IEEE Transactions on , Volume: 47 , Issue: 8 , Aug. 2000
Pages:1636 - 1644

[\[Abstract\]](#) [\[PDF Full-Text \(236 KB\)\]](#) IEEE JNL

8 The influence of localized states on gate tunnel currents-modeling and simulation

Wettstein, A.; Schenk, A.; Scholze, A.; Fichtner, W.;

Simulation of Semiconductor Processes and Devices, 1997. SISPAD '97., 1997 International Conference on , 8-10 Sept. 1997
Pages:101 - 104

[\[Abstract\]](#) [\[PDF Full-Text \(272 KB\)\]](#) IEEE CNF

9 Impact of high- κ dielectrics on undoped double-gate MOSFET scaling

Qiang Chen; Lihui Wang; Meindl, J.D.;

SOI Conference, IEEE International 2002 , 7-10 Oct. 2002
Pages:115 - 116

[\[Abstract\]](#) [\[PDF Full-Text \(245 KB\)\]](#) IEEE CNF

10 Modeling the limits of gate oxide scaling with a Schrodinger-based method of direct tunneling gate currents of nanoscale MOSFETs

Chung-Kuang Huang; Goldsman, N.;

Nanotechnology, 2001. IEEE-NANO 2001. Proceedings of the 2001 1st IEEE Conference on , 28-30 Oct. 2001
Pages:335 - 340

[\[Abstract\]](#) [\[PDF Full-Text \(449 KB\)\]](#) IEEE CNF

11 Simulation of direct tunneling through stacked gate dielectrics by a fully integrated 1D-Schrodinger-Poisson solver

Wettstein, A.; Schenk, A.; Fichtner, W.;

Simulation of Semiconductor Processes and Devices, 1999. SISPAD '99. 1999 International Conference on , 6-8 Sept. 1999
Pages:243 - 246

[\[Abstract\]](#) [\[PDF Full-Text \(260 KB\)\]](#) IEEE CNF

12 Noise modeling for RF CMOS circuit simulation

Scholten, A.J.; Tiemeijer, L.F.; van Langevelde, R.; Havens, R.J.; Zegers-van

Duijnhoven, A.T.A.; Venezia, V.C.;

Electron Devices, IEEE Transactions on , Volume: 50 , Issue: 3 , March 2003

Pages:618 - 632

[\[Abstract\]](#) [\[PDF Full-Text \(809 KB\)\]](#) [IEEE JNL](#)

13 Direct observation of secondary ionization current in n-channel MOSFETs

Mihnea, A.; Rudeck, P.J.; Chun Chen; Prall, K.D.; Ghodsi, R.;

Electron Devices, IEEE Transactions on , Volume: 49 , Issue: 12 , Dec. 2002

Pages:2301 - 2307

[\[Abstract\]](#) [\[PDF Full-Text \(379 KB\)\]](#) [IEEE JNL](#)

14 Voltage- and temperature-dependent gate capacitance and current model: application to ZrO/sub 2/ n-channel MOS capacitor

Yang-Yu Fan; Nieh, R.E.; Lee, J.C.; Lucovsky, G.; Brown, G.A.; Register, L.F.; Banerjee, S.K.;

Electron Devices, IEEE Transactions on , Volume: 49 , Issue: 11 , Nov. 2002

Pages:1969 - 1978

[\[Abstract\]](#) [\[PDF Full-Text \(509 KB\)\]](#) [IEEE JNL](#)

15 Model and analysis of gate leakage current in ultrathin nitrided oxide MOSFETs

Jonghwan Lee; Bosman, G.; Green, K.R.; Ladwig, D.;

Electron Devices, IEEE Transactions on , Volume: 49 , Issue: 7 , July 2002

Pages:1232 - 1241

[\[Abstract\]](#) [\[PDF Full-Text \(406 KB\)\]](#) [IEEE JNL](#)

[1](#) [2](#) [3](#) [4](#) [Next](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☒ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

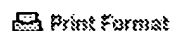
- ☐ By Author
- ☐ Basic
- ☐ Advanced

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE Enterprise

- ☐ Access the IEEE Enterprise File Cabinet



Print Format

Your search matched **5** of **1049776** documents.A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:

You may refine your search by editing the current search expression or entering a new one in the text box.

(resonant <and> tunneling <and> diodes:models) <in>

[Search](#)☐ Check to search within this result set

Results Key:

JNL = Journal or Magazine **CNF** = Conference **STD** = Standard**1 An improved multipeak resonant tunneling diode model for nine-state resonant tunneling diode memory circuit simulation***Chih Yuan Huang; Morris, J.E.; Yan Kuin Su;*

Electron Devices, IEEE Transactions on , Volume: 42 , Issue: 9 , Sept. 1995

Pages:1705 - 1707

[\[Abstract\]](#) [\[PDF Full-Text \(256 KB\)\]](#) **IEEE JNL****2 Resonant tunneling diodes: models and properties***Jian Ping Sun; Haddad, G.I.; Mazumder, P.; Schulman, J.N.;*

Proceedings of the IEEE , Volume: 86 , Issue: 4 , April 1998

Pages:641 - 660

[\[Abstract\]](#) [\[PDF Full-Text \(356 KB\)\]](#) **IEEE JNL****3 SPICE implementation of double barrier resonant tunnel diode model***Neculoiu, D.; Tebeanu, T.;*

Semiconductor Conference, 1996., International , Volume: 1 , 9-12 Oct. 1996

Pages:181 - 184 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(276 KB\)\]](#) **IEEE CNF****4 Combined self-consistent resonant-tunneling diode model***Abramov, I.I.; Goncharenko, I.A.;*

Microwave and Telecommunication Technology, 2001. CriMiCo 2001. 11th

International Conference on , 2001

Pages:443 - 444

[\[Abstract\]](#) [\[PDF Full-Text \(295 KB\)\]](#) **IEEE CNF****5 Large-signal resonant tunneling diode model for SPICE3 simulation***Kuo, T.-H.; Lin, H.C.; Anandakrishnan, U.; Potter, R.C.; Shupe, D.;*

Electron Devices Meeting, 1989. Technical Digest., International , 3-6 Dec. 1989

Pages:567 - 570

[\[Abstract\]](#) [\[PDF Full-Text \(208 KB\)\]](#) **IEEE CNF**